AMENDMENTS TO THE CLAIMS

1.-2. (Canceled)

3. (Currently Amended) The electronic circuit according to claim 18, wherein said central processing unit, said peripheral unit, said synchronization means, said data bus and said oscillator are arranged on [[a]] the common chip card.

4. (Previously Presented) The electronic circuit according to claims 18 , wherein said central processing unit, said peripheral unit, said data bus, said controllable oscillator and said synchronization means are integrated into an integrated circuit.

5. (Previously Presented) The electronic circuit according to claim 18, further comprising:

controlling means having a control output, said control output being connected to said control input of said controllable oscillator, and said controlling means being arranged to control said controllable oscillator depending on a control parameter.

6. (Previously Presented) The electronic circuit according to claim 5, wherein said controlling means is arranged to control said controllable oscillator depending on energy available for said electronic circuit such that the energy available for said electronic circuit is distributed to the peripheral unit and the central processing unit.

7. (Previously Presented) The electronic circuit according to claim 18, wherein said controllable oscillator is controllable to provide an output signal at a signal output, the frequency of which is faster than a frequency of a clock signal which can be fed to said clock connection of said central processing unit.

8. (Previously Presented) The electronic circuit according to claim 18, wherein said controllable oscillator is controllable to provide an output signal, the

frequency of which has no common divisor with a frequency of a clock signal which can be fed to said clock connection of said central processing unit.

9. (Previously Presented) The electronic circuit according to claim 18, being embodied as a cryptography controller.

10. (Previously Presented) The electronic circuit according to claim 18, wherein said peripheral unit is one of a coprocessor for a cryptographic algorithm including an asymmetrical encrypting or a symmetrical encrypting, a hash module, or a random generator.

11. (Previously Presented) The electronic circuit according to claim 18, comprising a plurality of peripheral units, each peripheral unit being connectable to a separate controllable oscillator, or wherein clock signals with frequencies are fed to various of said plurality of peripheral units, these frequencies being derived from said controllable oscillator.

12. (Previously Presented) The electronic circuit according to claim 11, wherein a separate task is associated to each peripheral unit, the tasks being selected from a group including computing a modular multiplication, a modular addition, a hash value computation, an RSA encrypting, an encrypting based on elliptical curves, an encrypting according to the DES standard, a data exchange with a terminal, forming random numbers or checking safety-critical parameters.

13. (Currently Amended) A method of controlling an electronic circuit having a central processing unit (CPU) and a peripheral unit being connected to each other via a data bus, wherein said central processing unit and said peripheral unit are arranged on a common chip card, comprising:

clocking said central processing unit by a first clock using an external connection device of the common chip card, being arranged to be connectable to a corresponding contact connection of a terminal;

clocking said peripheral unit by a second clock using a controllable oscillator of the electronic circuit, the controllable oscillator being controlled independent from the first clock; ~~and~~

synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus; and

controlling said controllable oscillator depending on energy available for said electronic circuit such that the energy available for said electronic circuit is distributed to the peripheral unit and the central processing unit, and a computing speed with the energy available for said electronic circuit is maximized.

14. (Previously Presented) The electronic circuit according to claim 18, wherein said clock connection is connected to the signal output of the controllable oscillator, so that the second clock is adjustable such that the second clock is – irrespective of the unit used for representing the frequencies of the first and the second clocks - relatively prime with respect to the first clock.

15.-17. (Canceled)

18. (Currently Amended) An electronic circuit, comprising:

a central processing unit having a clock connection for receiving a first clock and a data connection;

a peripheral unit having a clock connection and a data connection;

synchronization means comprising a first and a second data connection, said first data connection being connected to said data connection of said peripheral unit; and

a data bus being connected to said data connection of said central processing unit and to said second data connection of said synchronization means,

wherein said central processing unit, said peripheral unit, said synchronization means, said data bus and [[said]] an oscillator are arranged on a common chip card, said clock connection of said peripheral unit is connected to said signal output of said controllable oscillator, said clock connection of said central processing unit is coupled to an external connection device being arranged to be connectable to a corresponding contact connection of a terminal, and said controllable oscillator being controlled independent from the first clock,

a controlling means being arranged to control said controllable oscillator depending on energy available for said electronic circuit such that the energy available for said electronic circuit is distributed to the peripheral unit and the central processing unit, and a computing speed with the energy available for said electronic circuit is maximized.